multiplexer circuit is set to output the frame data according to a "selected active link width" specified in a received link management packet. In fact, Parthasarathy et al. provides no description whatsoever of a multiplexer configured for switching between ***a prescribed maximum link width*** and a ***selected active link width***, as claimed.

In fact, the cited portion of column 9, line 55 through col. 10, line 65 provides no description of any link layer operations. Rather, col. 9, line 55 to col. 10, line 65 of Parthasarathy et al. simply provides a description of the host channel adapter (HCA) (i.e., host fabric adapter) 120 Figure 7, where a micro-engine 710 is "utilized to build, send, receive and acknowledge NGIO/InfiniBand™ cells between the host memory 206 (see FIG. 6) and a serial link" (col. 9, lines 49-52), where the micro-engine 710 coordinates send queue and receive queue operations (e.g., col. 9, line 64 to col. 10, line 5).

In addition, column 10, lines 17-31 simply describes a context memory interface 716 that "provides an interface to a context manager (not shown) responsible for providing the necessary context for a work queue pair (WQP) used for sending and receiving a NGIO/InfiniBand™ cell/packet" (col. 10, lines 17-20). Column 10, lines 32-41 provide a summary description of a local bus interface 718 interfacing to a local data bus, and a completion queue/doorbell manager interface 720 providing an interface to completion queues.

In fact, Parthasarathy et al. teaches no more than sending and receiving data packets through a FIFO interface 722 at col. 10, lines 41-57, where packets are simply "processed" and sent and/or received to the switch fabric 100' via a serial interface 730.

Hence, the description of the host-fabric adapter 120 of Figure 7 provides no description of any link layer operations, let alone any multiplexer configured for selectively switching frame data ***from a prescribed maximum link width*** to a transmit bus according to ***a selected active link width***, as claimed.

Further, Figures 2 and 5-6 provide no description or suggestion of any link layer operations, let alone any multiplexer configured for switching frame data "of ***a prescribed maximum link width***" to a selected active link width, as claimed. Rather, Figure 2 simply describes a data network having a host system including the host channel adapter 120 (already

described above with respect to Figure 7) (col. 2, lines 46-49; col. 4, line 46 to col. 6, line 4); Figure 5 describes a software driver stack for the operating system of the host system and that includes the host channel adapter 120 of Figure 7 (col. 2, lines 57-59; col. 6, line 38 to col. 8, line 36); and Figure 6 describes the host system 130 and includes the host channel adapter 120 of Figure 7 (col. 8, line 37 to col. 9, line 24).

Applicant strenuously traverses in the unfounded assertions in the rejection: Parthasarathy et al. provides no reference whatsoever to any "Management Datagram (MAD)", "Subnet Management Packets (SMP)", or "Active Link Width", as asserted. Further, Parthasarathy et al. provides no description whatsoever of any multiplexer circuit that selectively switches frame data of a prescribed maximum link width to a selected one of a plurality of available link widths: as described above, the cited col. 10, lines 16-64 provides no description whatsoever of any link layer operations: in fact, Parthasarathy et al. provides no reference to the claimed term "link width"!

Hence, the unfounded assertions by the Examiner cannot overcome the deficiencies of the reference, because "[a] prior art patent is a reference only for that which it teaches." Corning Glass v. Sumitomo Electric, 9 USPQ2d 1962, 1970 (Fed. Cir. 1989).

Applicants further traverse the ill-founded assertion that Parthasarathy et al. teaches "multiplexing means for combining packets of VL 0-15" as a disclosure of the claimed multiplexer circuit that selectively switches ***frame data of a prescribed maximum link width*** to a ***selected active link width***: the rejection assumes facts not in evidence, namely that Figure 6 discloses virtual lanes (VL) 0-15, when in fact Parthasarathy et al. provides no reference whatsoever to any "virtual lane" or "VL"!

Further, even if Parthasarathy et al. described a "virtual lane", the broadest reasonable interpretation of the claimed "link width" cannot be so broadly construed as to encompass ***virtual lanes*** (VLs), because such an interpretation would be inconsistent with the specification.

The specification explicitly distinguishes between virtual lanes and link widths: the specification describes that virtual lanes are serviced by a virtual lane arbitration module 64 (see Fig. 2) which determines "which virtual lane to service, in what order, and for what duration"

(page 5, lines 20-24); in contrast, the specification describes that the multiplexer 76 of Figs. 2 and 3 is used to select a ***link width*** for transmission of the frame data (supplied at ***the maximum link width***) to a physical network link that is connected to the channel adapter port, where:

> The multiplexer 76, controlled by the link send engine 62, is used to select a link width of the port. In particular, the multiplexer 76 is used to enable selection of 1x, 4x, and 12x link widths according to the InfiniBand™ Specification. The link send engine 62, also referred to as a bus controller, determines the selected active link width based on reading the link width active field 18b in the port info table 18 during initialization. ***The bus controller 62 sets the multiplexer circuit 76 to switch the frame data according to the selected active link width***. The bus controller 62 also is configured for outputting ***sequencing signals for controlling the sequence of outputting frame data units onto the link 16 when the link 16 is less than the prescribed maximum link width*** (e.g., 16x).
>
> (page 6, lines 6-13; see also page 7, lines 7-25).

Hence, the specification explicitly distinguishes between virtual lanes and link widths by specifying that the link width refers to the width of the actual width of the physical interface link (see also page 4, lines 4-11).

Further, Parthasarathy et al. also distinguishes between virtual lanes and "physical links" noting that "[e]ach physical link may support a number of logical point-to-point channels." (Column 4, lines 1-3).

Hence, interpreting the claimed "link widths" as reading on virtual lanes would be inconsistent with the specification in Parthasarathy et al., and therefore unreasonable.[1]

Further, the rejection fails to demonstrate that the applied reference inherently requires

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[1]"During patent examination, the pending claims must be 'given their broadest reasonable interpretation consistent with the specification.'" MPEP §2111 at 2100-46 (Rev. 3, Aug. 2005) (*quoting In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000)).

"The broadest reasonable interpretation of the claims must also be consistent with the interpretation that those skilled in the art would reach." MPEP §2111.01 at 2100-47 (Rev. 3, Aug. 2005) (*citing In re Cortright*, 165 F.3d 1353, 1359, 49 USPQ2d 1464, 1468 (Fed. Cir. 1999)).

use of a multiplexer.[2] In fact, numerous variations may be implemented for responding to a link management packet, including implementing multiple link transceivers having respective data rates, where only one of the link transceivers is selected based on the corresponding link width specified in the received link management packet; hence, if a link management packet specifies a ""4x" link width, one possible implementation would be for the channel adapter to enable the "4x" transceiver and disable the remaining transceivers (e.g., the "1x" transceiver and the "12x" transceiver).

In contrast, each of the independent claims specify the multiplexer circuit configured for "selectively ***switching*** frame data of a prescribed maximum link width". As described in the specification, the "switching" in the multiplexer of Figure 3 includes not only transfer of data, but transfer of the data according to the appropriate width, and the appropriate sequence for transmissions using link widths smaller than the prescribed maximum link width:

> The switch 96 is configured for switching the frame data according to the selected active link width specified in the link width active register 18b based on the switching control signal 106 from the bus controller 62. Hence, the multiplexer circuit 76 may output ***twelve (12) hyperbytes in sequence*** for a 1x link, or ***three (3) 4-hyperbyte groups in sequence*** for a 4x link. In the case of a 12x link that corresponds to the prescribed maximum link width, the switch 96 selects a 108-bit bypass bus 110 that bypasses the multiplexer circuitry.
>
> (Page 7, lines 1-6).

Hence, the rejection should be withdrawn because it fails to demonstrate that the applied reference discloses each and every element of the claim. See MPEP 2131. "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v.*

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[2]See MPEP 2112 ("The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993)(reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); ... 'The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" (quoting In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999))).

Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). "Anticipation cannot be predicated on teachings in the reference which are vague or based on conjecture." *Studiengesellschaft Kohle mbH v. Dart Industries, Inc.*, 549 F. Supp. 716, 216 USPQ 381 (D. Del. 1982), *aff'd.*, 726 F.2d 724, 220 USPQ 841 (Fed. Cir. 1984).

In view of the above, it is believed this application is in condition for allowance, and such a Notice is respectfully solicited.

To the extent necessary, Applicant petitions for an extension of time under 37 C.F.R. 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including any missing or insufficient fees under 37 C.F.R. 1.17(a), to Deposit Account No. 50-0687, under Order No. 95-520, and please credit any excess fees to such deposit account.

Respectfully submitted,

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